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Ultra-thick metal ohmic contact fabrication using surface activated bonding

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We successfully bonded aluminum foils to Si substrates to fabricate p-Si/Al, n-Si/Al, p^+-Si/Al, and n^+-Si/Al junctions by surface activated bonding (SAB). The effects of the annealing temperature process on the electrical properties of the junctions were investigated by measuring their current voltage (*I-V*) characteristics. It was found that the leakage current of the reverse bias of n-Si/Al junctions was improved and the *I-V* characteristics of p-Si/Al revealed excellent linearity properties after the junctions annealing at 400 °C. The interface resistance of p^+-Si/Al, and n^+-Si/Al junctions decreased with increasing annealing temperature and decreased to 0.021 and 0.032 $\Omega \cdot cm^2$ after the junction annealing at 300 and 400 °C, respectively. These results demonstrated that thick metal Ohmic contact in devices could be realized by SAB.

Introduction

Ohmic contact to semiconductor substantially degrades the overall performance of the high-power devices and circuits with large-current and/or high-voltage capability (1). The major loss of performance is usually due to high ohmic contact resistance between metal electrode and semiconductor. Thus, the realization of excellent ohmic contact on semiconductor is absolutely necessary to obtain optimum device performance. The primary factors determining contact resistance are carrier concentration, semiconductor surface preparation and cleaning, and contact metal work functions hence Schottky barrier height (2, 3). In addition, it was reported that the ohmic contact resistance decreased with increasing the metal thickness.[4] However, the deposition of a thick metal layer is extremely difficult to obtain because it would take a large quantity of time and the production cost by the conventional coating method such as Electron-Beam-Evaporation and Sputter-Deposition. On way to circumvent these difficulties is surface-activated bonding (SAB) (5, 6), in which different substrate materials could be directly bonded to each other without heating. We previously successfully fabricated p-Si/Al junctions and found that the current-voltage characteristics of the junctions revealed Schottky properties (7). The formation of Ohmic contact frequently requires a high temperature step so that the evaporated metals could alloy with the semiconductor to reduce the barrier height of the interface. Thus, the investigation of the annealing temperature-dependent electrical properties of Si/Al junctions is very important to realize the thick film metal contacts.

In this study, we demonstrated the fabrication of p-Si/Al, n-Si/Al, and p^+-Si/Al, and n^+-Si/Al junctions by SAB method and examined the annealing temperature dependence of the electrical properties of all the junctions. The electrical properties of the junctions without and with annealing were investigated by *I-V* measurements and the feasibility of the thick film metal contact was discussed. Furthermore, their interfaces were investigated by field emission-scanning electron microscopy (FE-SEM).

Experimental Process

Four types (p-, n-, p^+-, and n^+-) of (100) Si substrates and aluminum foils (Al) with a thickness of 38 μm (it is commercially available) are used for our bonding experiment. The carrier concentrations of Si substrates are shown in Table Ⅰ. The Al/Ni/Au and Ti/Au multilayers were evaporated on the back surfaces of p-Si and n-Si substrates prior to the bonding, respectively, and the Ohmic contacts of p-Si substrates were achieved by rapid thermal annealing at 400 °C for 1 min in N_2 gas ambient. Al foils were bonded to each Si substrates by using SAB (5, 6), so that p-Si/Al, n-Si/Al, p^+-Si/Al, and n^+-Si/Al foil junctions were obtained. In addition, p^+-Si and n^+-Si substrates with Al contacts on both surfaces were fabricated by deposition of 100 nm Al film on both surfaces of the substrates. The samples were not heated during the bonding process. After the bonding, a 4-by-6 mesa array was fabricated on the Al foils by using Al wet etching for 12 h. The wide and length of the mesa were all 1.4 mm. A top view photograph of the fabricated Si/Al junctions is shown in Figure 1a. An Agilent B2902A Precision Measurement Unit was used for measuring the *I-V* measurements of the junctions at different annealing temperature. The cross-sectional structures of Al/Si junctions were analyzed using an FE-SEM facility (JEOL JSM6500F).

TABLE I. The carrier concentration and the thickness of substrates.

Type	Carrier concentration (cm^{-3})	Thickness (μm)
p-Si (100)	2.4×10^{17}	525
n-Si (100)	8.5×10^{15}	525
p^+-Si (100)	2.6×10^{19}	525
n^+-Si (100)	2.6×10^{19}	525

Results and Discussion

We observed the microscopy images of the cross-section of the fabricated Si/Al junctions by using FE-SEM equipment. The observation results are shown in Figure. 1b. A straight line can be clearly recognized at the center of the junction, which corresponds to the bonded interfaces. Furthermore, no cracks or hollow spaces were observed at the bonded interface. This indicate that Al foils were firmly bonded to the Si substrates. The *I-V* characteristics of n-Si/Al junctions as a Schottky diode measured at room temperature are shown in Figure 2(a). Their *I-V* characteristics showed rectification properties. The ideality factor for the forward bias voltages between 0.1 and 0.3 V was calculated to be 2.08, 2.15, 2.14, 2.07, and 2.24 for the junction without and with annealing at 100, 200, 300, and 400 °C, respectively. The value is insensitive to the annealing temperature, which is larger than 2 suggesting that the recombination current mechanism mainly dominates the transport properties of carriers across the junction interface. We observed

that the magnitude of the forward bias current decreased as the annealing temperature increased, which should be attributed to the oxidation of the Al foils for the highr annealing process. In addition, the magnitude of the current at – 3 V significantly decreased from 2.7×10^{-2} to 5.0×10^{-4} A/cm^2 as the annealing temperature increased to 400 °C. The obtained values of parameter for the respective junctions are summarized in Table Ⅰ. Note that the reveres bias current continuously increased as the reverse bias voltage increased.

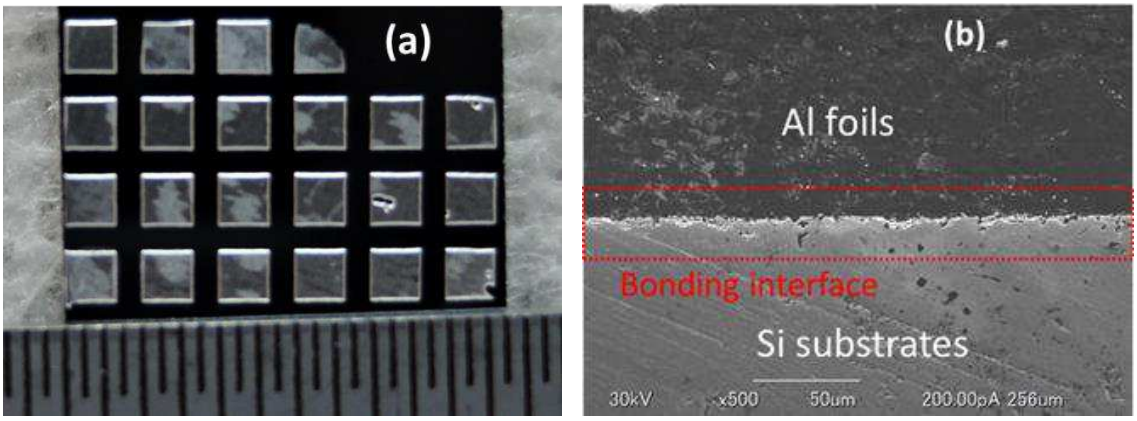

Figure 1. (a) A top view photograph of and (b) An FE-SEM cross-sectional image of the bonded Si/Al junctions.

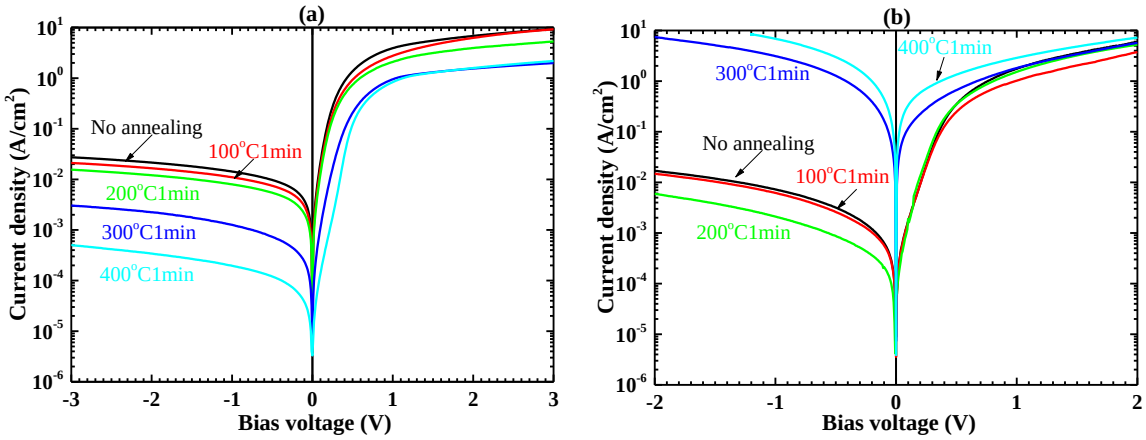

Figure 2. *I-V* characteristics of (a) n-Si/Al foil and (b) p-Si/Al junctions without and with annealing at 100, 200, 300, and 400 °C measured at room temperature.

Table Ⅱ. The reverse-bias current and ideality factor of n-Si/Al junctions and the interface resistance of p-Si/Al junctions

	n-Si/Al junction		p-Si/Al junction
Annealing temperature	**Reverse-bias current (A/cm^2)**	**Ideality factor**	**Resistance (Ω·cm^2)**
Without annealing	2.7×10^{-2}	2.08	102.04
100 °C	2.1×10^{-2}	2.15	109.89
200 °C	1.6×10^{-2}	2.14	178.57
300 °C	3.0×10^{-3}	2.07	0.73
400 °C	5.0×10^{-4}	2.24	0.26

The influence of the annealing temperature on the *I-V* characteristics of p-Si/Al junctions measured at room temperature is shown in Figure 2(b). We found that the *I-V* characteristics of the junction without annealing shown in this figure revealed Schottky rectification properties. The current density of the revere bias voltage decreased as the annealing temperature increased up to 200 °C and then increased after the annealing temperature increased from 300 to 400 °C. Moreover, the *I-V* characteristics of the junctions with annealing at 300 and 400 °C show linear property. The interface resistances were extracted to be 0.73 and 0.26 $\Omega \cdot cm^2$ for the junction annealed at 300 and 400 °C, respectively, by least-square fitting around 0 V. Similarly, the interface resistances of the junctions without and with annealing at 100 and 200 °C were calculated and the results are shown in Table Ⅰ. It was found that the interface resistance decreased with increasing the annealing temperature. Furthermore, the junction after annealing at 400 °C brought about the smallest value of the interface resistance in all the samples. However, this value is two orders of magnitude larger than the resistance of p-Si substrate (not shown in this paper) Ohmic contacts.

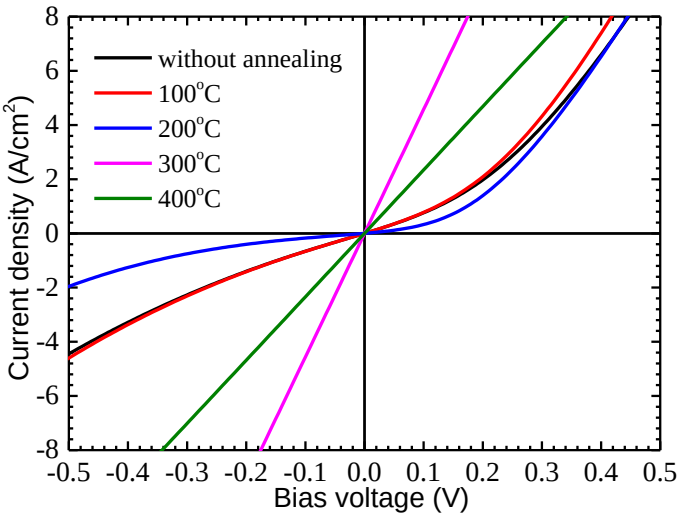

Figure 3. *I-V* characteristics of p^+-*Si/Al* foil junctions without and with annealing at 100, 200, 300, and 400 °C measured at room temperature.

The *I-V* characteristics of p^+-*Si/Al* foil junctions without and with annealing from 100 to 400 °C measured between - 0.5 and 0.5 V at room temperature are shown in Figure 3. We found that, in the bias voltage for the measurements, the *I-V* characteristics of p^+-*Si/Al* foil junctions without and with annealing at 100 and 200 °C showed nonlinear properties. However, after the junctions annealing at 300 and 400 °C their *I-V* characteristics show excellent linearity. Furthermore, their interface resistances were found to be 0.021 and 0.042 $\Omega \cdot cm^2$, respectively, by least-square fitting at approximately 0 V. In the same way, the resistances of the junctions with other various annealing temperature are obtained and shown in Figure 5. It was found that the interface resistance increased slightly as the annealing temperature increased up to 200 °C, and then decreased sharply as the annealing temperature increased to 300 °C, finally increased again when the temperature increased to 400 °C.

Figure 4 shows the *I-V* characteristics of n^+-Si/Al foil junctions without and with annealing from 100 to 600 °C measured between - 0.5 and 0.5 V at room temperature. It

was found that the *I-V* characteristics in this figure showed excellent linear property. By least-squares fitting at approximately 0 V, the interface resistance of the junctions without and with annealing at 100, 200, 300, 400, 500, 600 °C were determined to be 0.04, 0.042, 0.038, 0.036, 0.032, 0.060, 0.167 Ω·cm^2, respectively, and are shown in Figure 6. It is evident that the interface resistance decreases little by little with the annealing temperature increasing to 400 °C. Moreover, the junctions after annealing at 400 °C showed the smallest interface resistance among all n$^+$-Si/Al foil junctions. However, when the annealing temperature exceeded 400 °C, the interface resistance substantially increased.

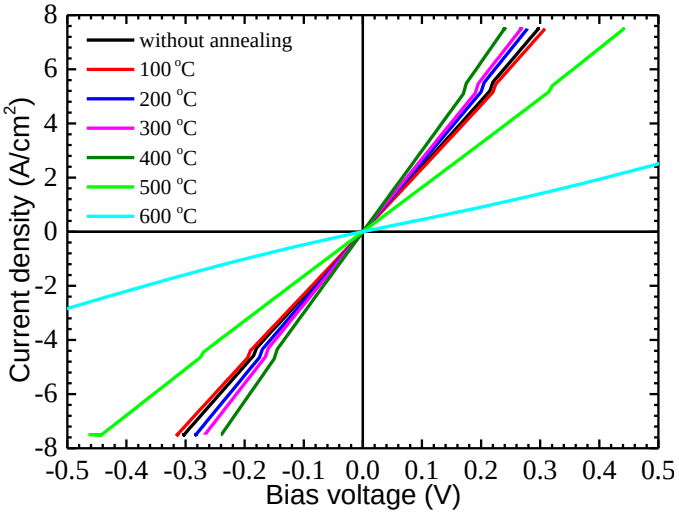

Figure 4. *I-V* characteristics of (a) n$^+$-Si/Al foil junctions and (b) n$^+$-Si substrates with Al contacts on both surfaces without and with annealing at 100, 200, 300, and 400 °C measured at room temperature.

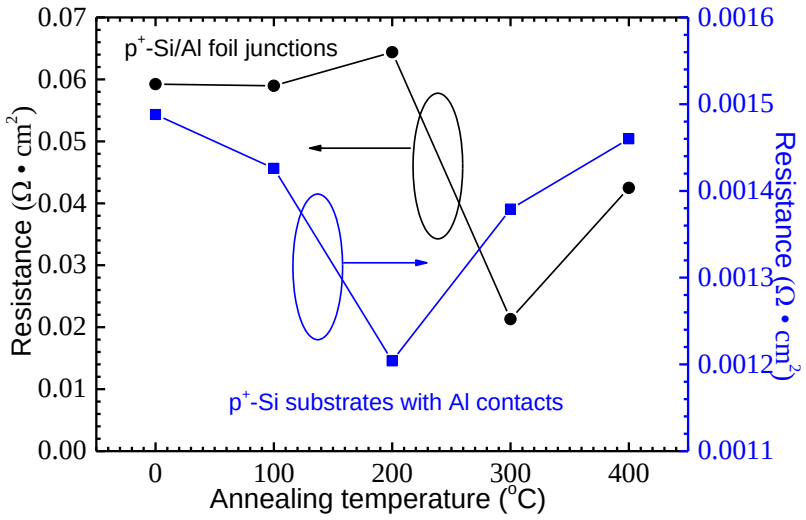

Figure 5. Resistances of the respective samples at various annealing temperatures for p$^+$-Si/Al foil junctions and p$^+$-Si substrates with Al contacts on both surfaces.

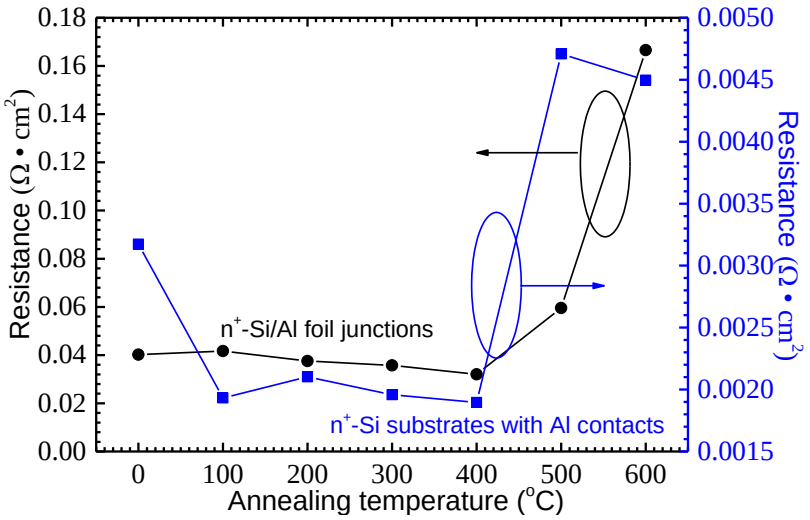

Figure 6. Resistances of the respective samples at various annealing temperatures for n^+-Si/Al foil junctions and n^+-Si substrates with Al contacts on both surfaces.

Discussion

It was found that the *I-V* characteristics of n-Si/Al, p-Si/Al, p^+-Si/Al, and n^+-Si/Al junctions largely depended on the annealing temperature. The reverse bias current of n-Si/Al junctions decreased as the annealing temperature increased. In contrast the current of p-Si/Al junctions markedly increased when the temperature is higher than 200 °C. With increasing the annealing temperature, the interface resistances of p^+-Si/Al and n^+-Si/Al junctions became more and more small. An upward trend in the resistance of p^+-Si/Al junctions with annealing at 300 °C was observed, which is due to the oxidation of Al foil surfaces for the high temperature annealing. Similar results were also observed in the contact resistance of p^+-Si substrates with Al film on both surfaces with annealing at various temperatures. The annealing temperature dependence of the ohmic contacts of p^+-Si substrates with Al film is shown in Figure 5. In addition, the interface resistance of n^+-Si/Al junctions continually decreased as the annealing temperature increased up to 400 °C and then increased as the annealing temperature increased to 600 °C. A similar change was observed in the contact resistance of n^+-Si substrates with Al film on both surfaces. The contact resistances of n^+-Si substrates with annealing at various temperatures are shown in Figure 6. In addition, the electrical conductivity of n^+-Si/Al junctions degraded at higher than 400 °C, which may be due to aluminum as acceptor impurities diffuses into n^+-Si substrates and causes the neutralization of acceptor and donor impurities near the bonded interfaces. A similar behavior has also been reported in multi-crystalline silicon (8).

The abovementioned the electrical conductivity of all the samples were improved after the junctions annealing at high temperature, which should be attributed to the recovery of the interface damaged layers due to the annealing process. In the bonding process, the Ar atom fast beam irradiation are used to the activation of substrate surfaces so that the amorphous layer with a thickness of several nanometers are formed on the bonding surface (9, 10). A large number of interface states should be existed at the bonding interface and distributed in the amorphous layer according to our previous report

(11, 12), which could directly act as traps and recombination centers. Such interface states can introduce a large charge at the interface so that a potential barrier and depletion layers form in the conduction band (valence band) of Si/Al bonded interface. It was reported that the thickness of the amorphous layers and the density of interface states depended on the annealing temperature in Si/Si junctions fabricated by SAB, which decreased as the annealing temperature increased (12). Furthermore, the electrical conductivity of Si/Si junctions was significantly improved after annealing at high temperature. Consequently, the high annealing process larger than 400 °C is essential for obtaining low interface resistance of p-Si/Al junctions. These results suggest that the bonding processes of thick metal foil has the potential of providing low resistance Ohmic contacts and reducing the fabrication cost of devices.

Conclusion

We fabricated the n-Si/Al, p-Si/Al, n^+-Si/Al, and p^+-Si/Al junctions using SAB method and demonstrated the influence of thermal annealing process on their electrical properties. The *I-V* characteristics of the n-Si/Al junctions after annealing at 400 °C showed good rectification properties. In contrast, the *I-V* characteristics of p-Si/Al junction with annealing at 400 °C revealed linear properties. Moreover, the interface resistance of 0.26 $\Omega \cdot cm^2$ was obtained. The interface resistance of n^+-Si/Al and p^+-Si/Al junctions decreased with a rise in the annealing temperature. They were reduced to 0.032 and 0.021 $\Omega \cdot cm^2$ after the junction annealing at 400 and 300 °C, respectively. These results indicate that SAB of metal foils is an effective way for fabricating thick film electrode with a thickness of several-ten micrometers.

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